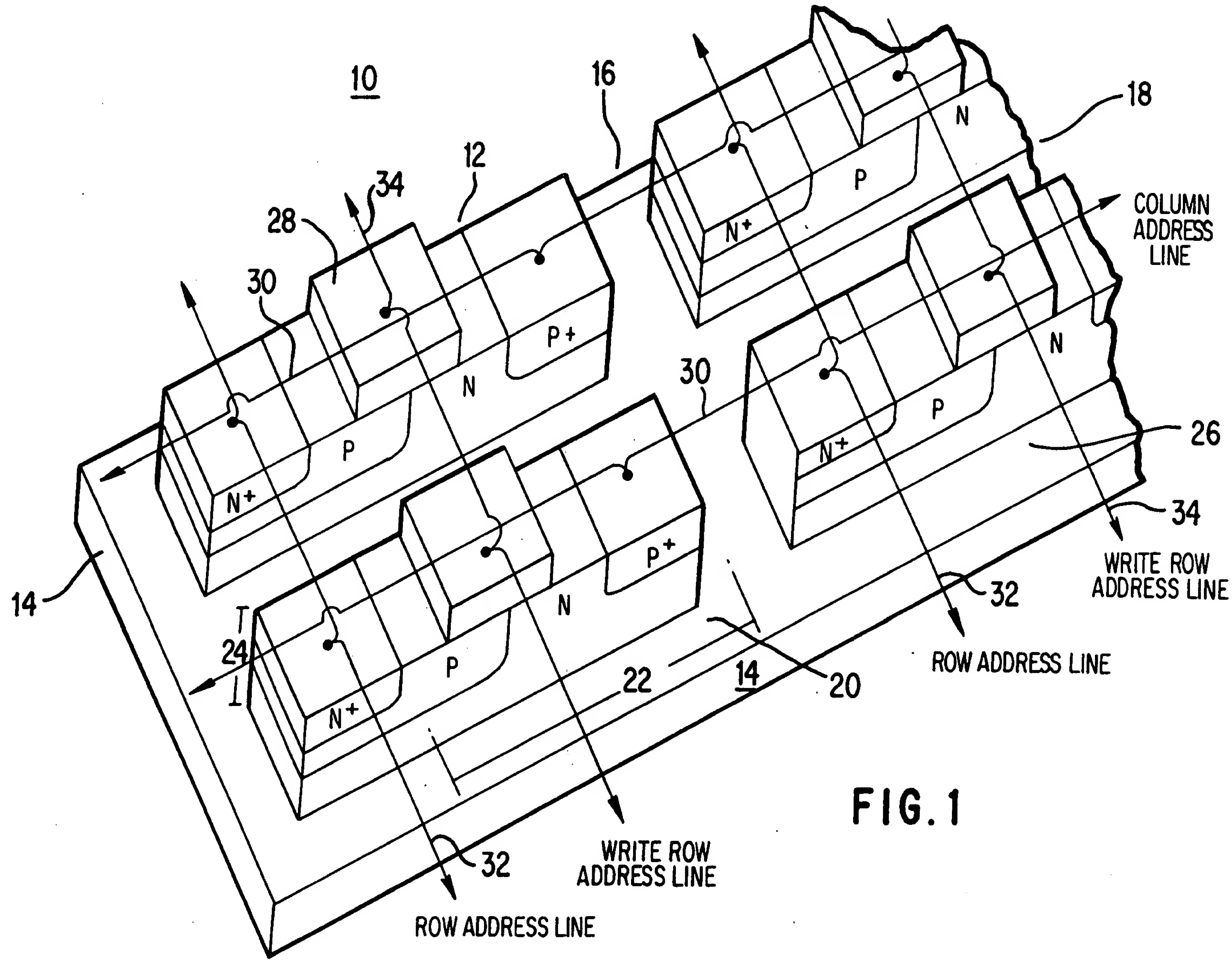
10
16
12
34
28
30
18
COLUMN
ADDRESS
LINE
N
P
N+
P+
30
26
34
WRITE ROW
ADDRESS LINE
32
ROW ADDRESS LINE
14
24
22
14
20
32
WRITE ROW
ADDRESS LINE
ROW ADDRESS LINE

FIG. 1

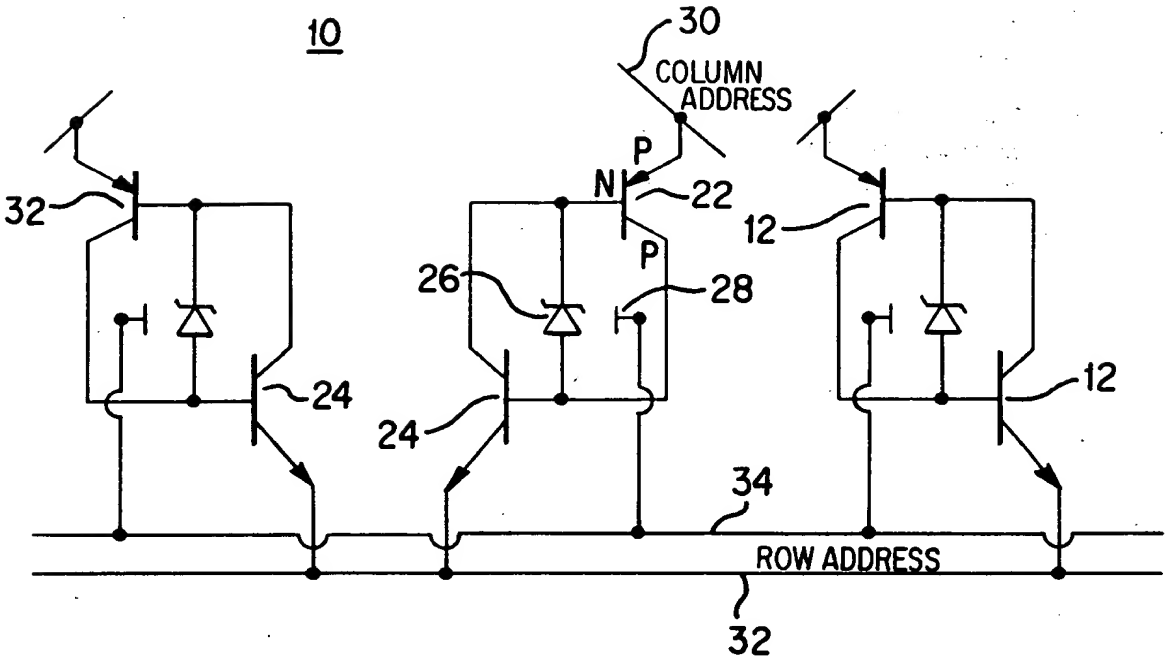
10
30
COLUMN
ADDRESS
P
N
22
32
12
P
26
28
24
12
24
34
ROW ADDRESS
32

FIG. 2

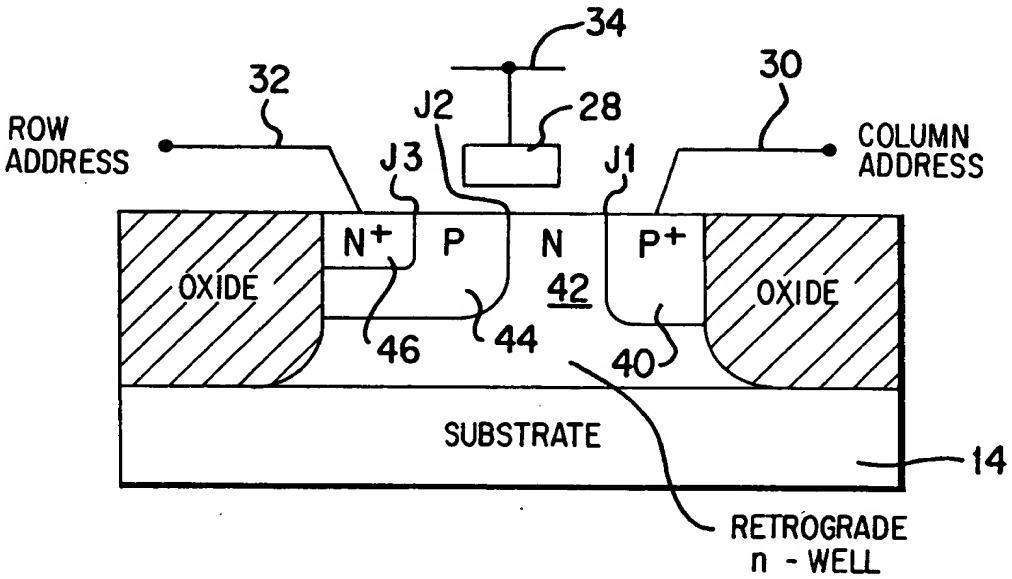
34
32
30
J2
28
ROW
ADDRESS
J3
J1
COLUMN
ADDRESS
N+
P
N
P+
OXIDE
42
OXIDE
46
44
40
SUBSTRATE
14
RETROGRADE
n - WELL

FIG. 3

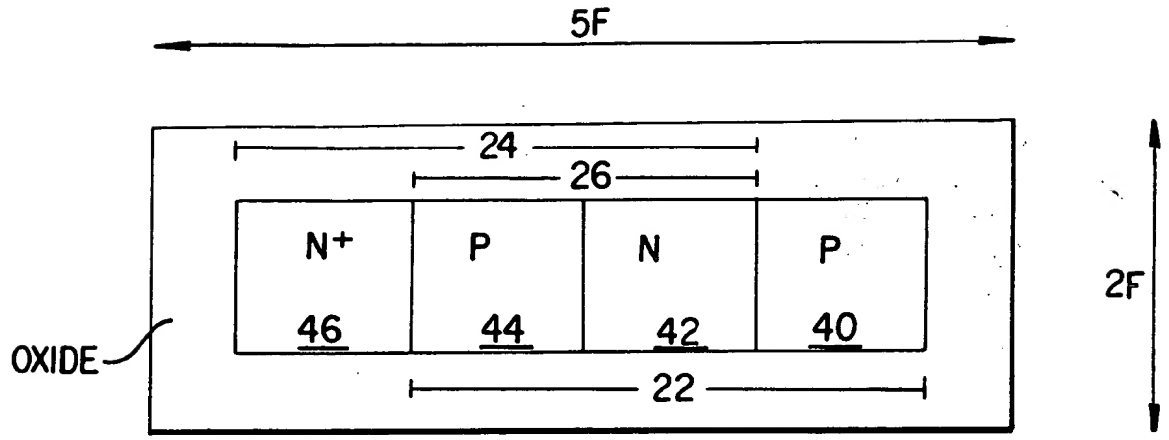

FIG. 4

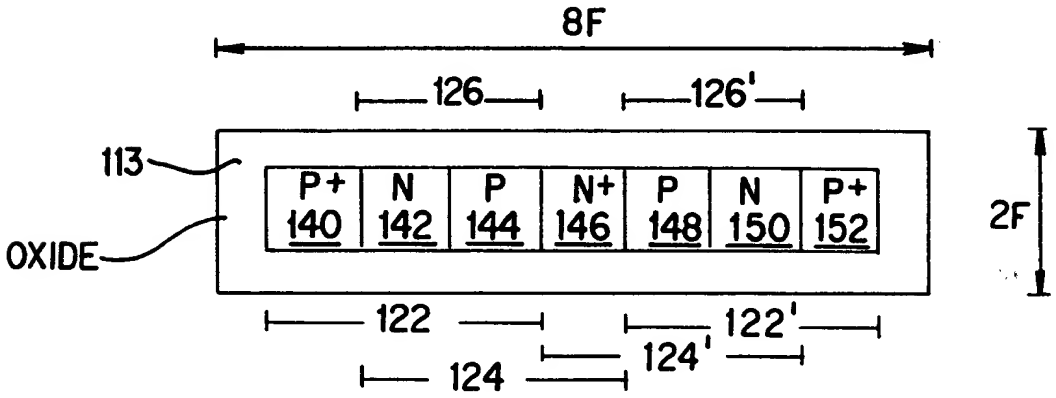

FIG. 14

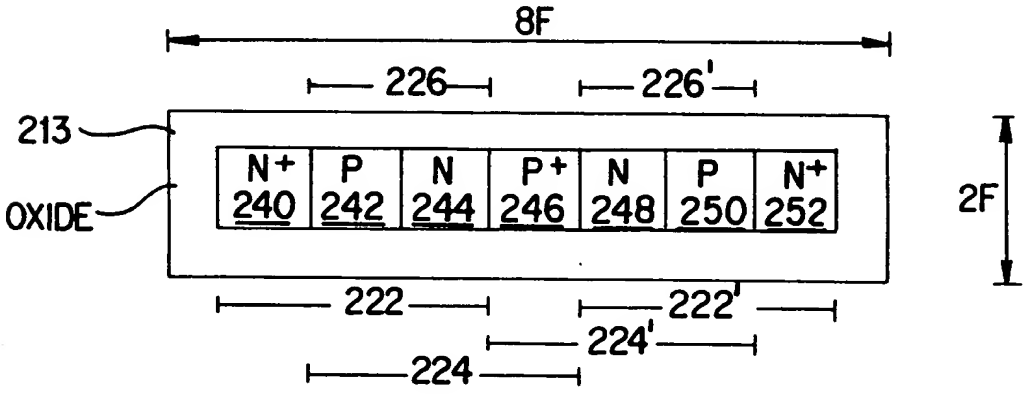

FIG. 17

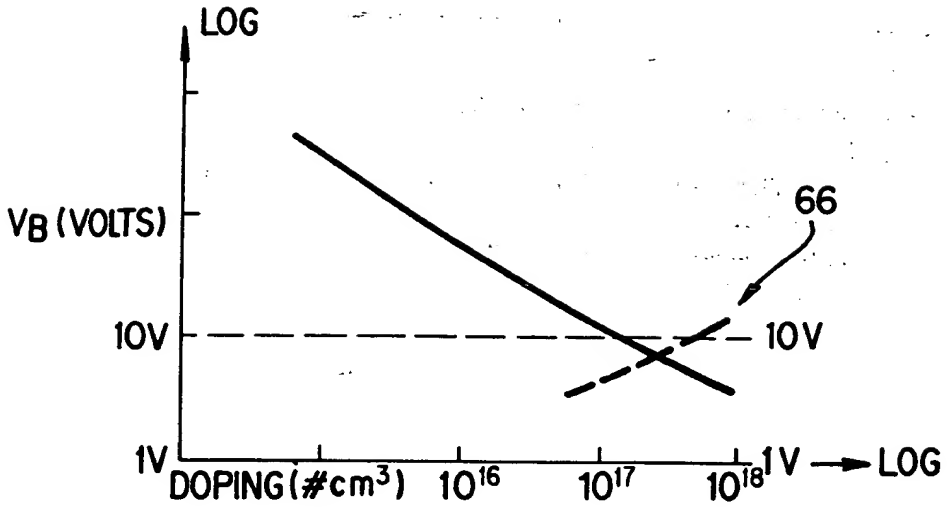
LOG
V_B (VOLTS)
66
10V
10V
1V
DOPING (#cm^3)
10^{16}
10^{17}
10^{18}
1V → LOG

FIG. 5

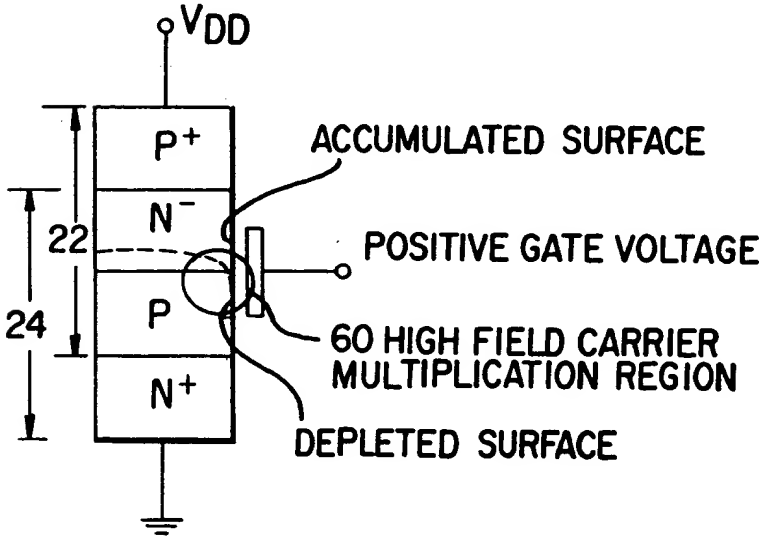
V_{DD}
P^+
N^-
P
N^+
22
24
ACCUMULATED SURFACE
POSITIVE GATE VOLTAGE
60 HIGH FIELD CARRIER MULTIPLICATION REGION
DEPLETED SURFACE

FIG. 6

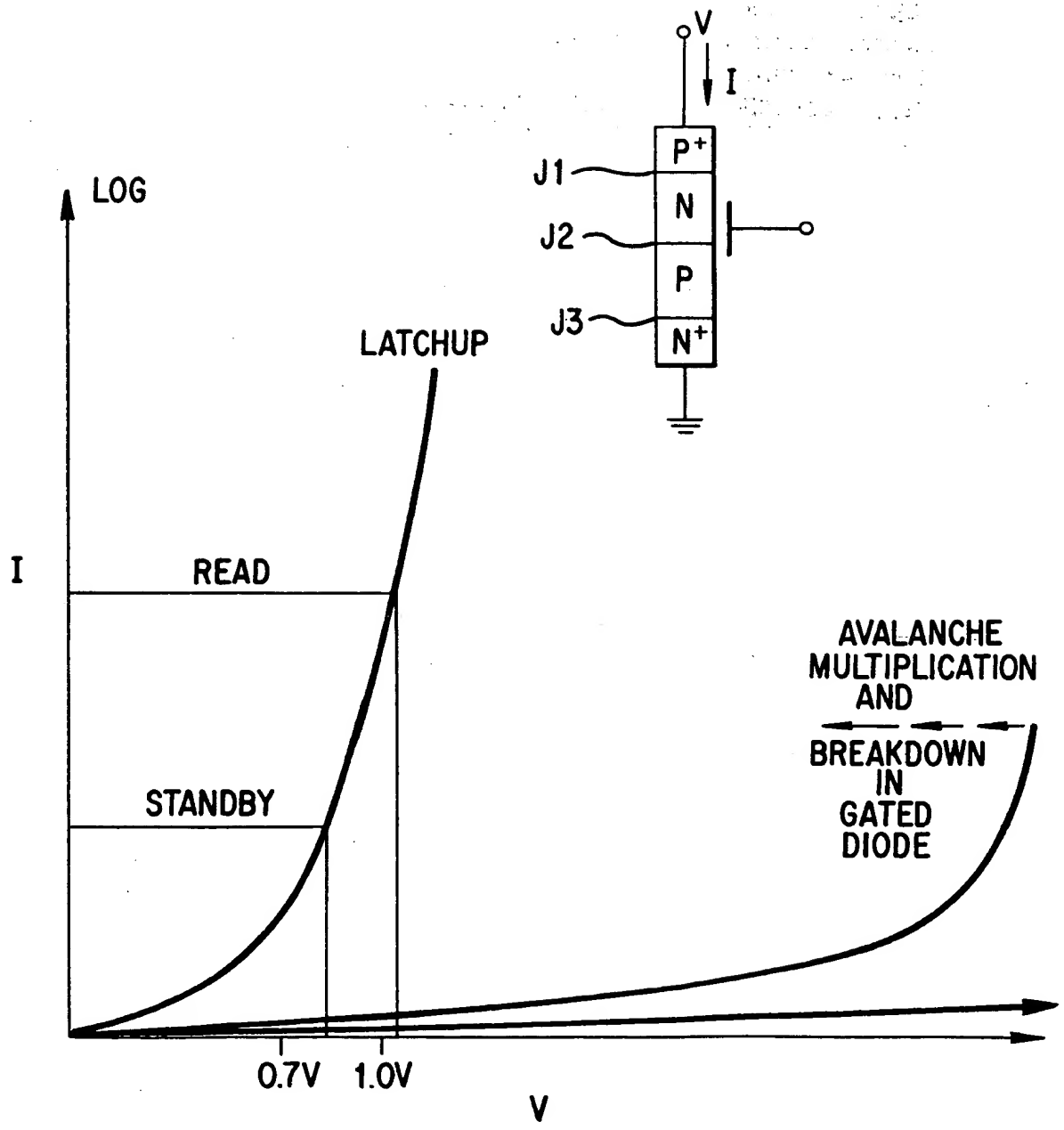
V
I
P+
N
P
N+
J1
J2
J3
LOG
I
LATCHUP
READ
STANDBY
AVALANCHE
MULTIPLICATION
AND
BREAKDOWN
IN
GATED
DIODE
0.7V
1.0V
V

FIG. 7

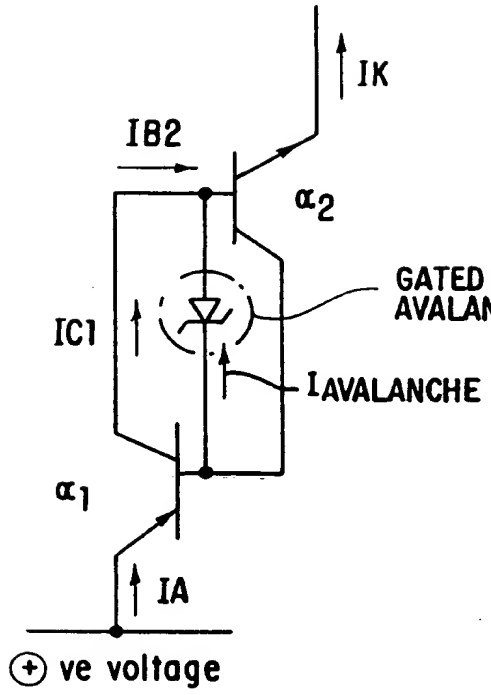
IK
IB2
α_2
GATED DIODE AVALANCHE
IC1
$I_{AVALANCHE}$
α_1
IA
⊕ ve voltage

FIG. 8

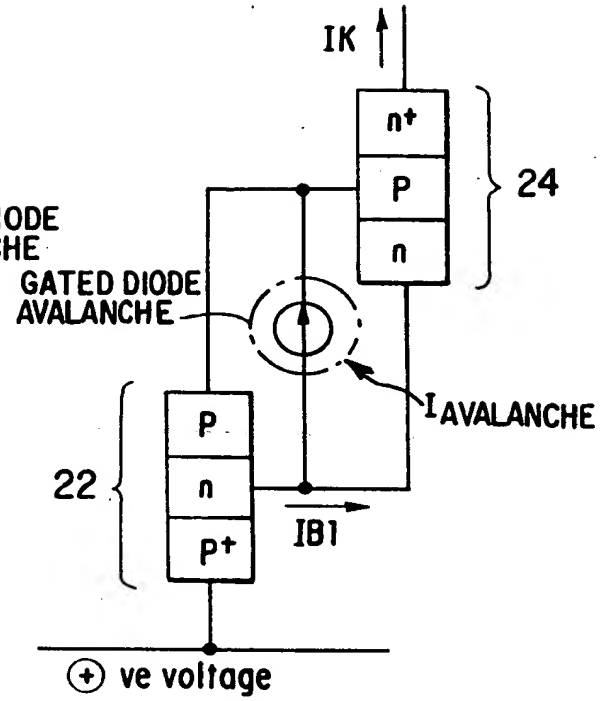
IK
n+
P
n
24
GATED DIODE AVALANCHE
$I_{AVALANCHE}$
P
n
P+
22
IB1
⊕ ve voltage

FIG. 9

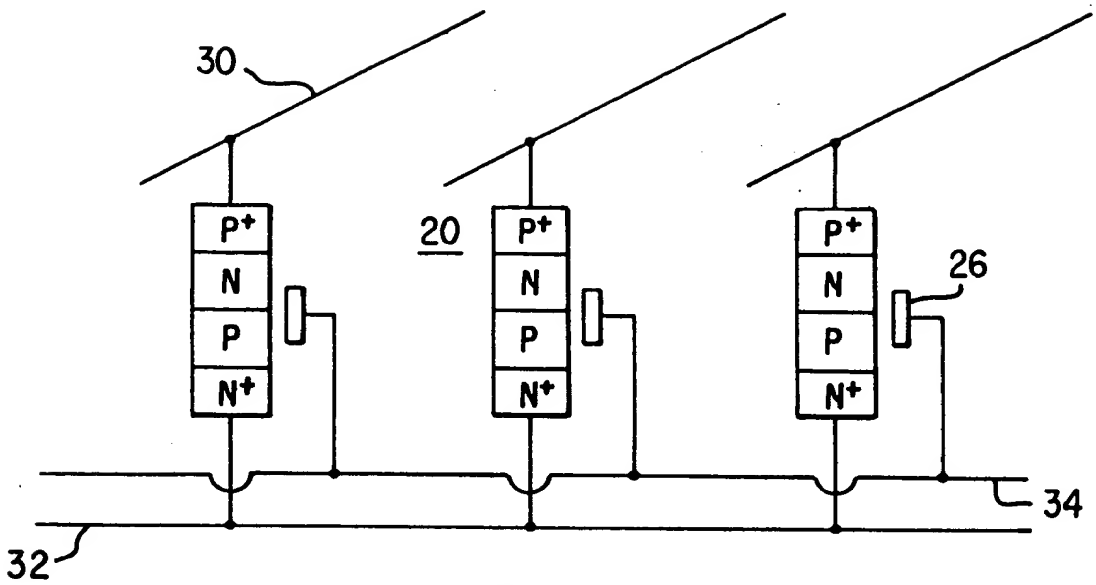

FIG. 10

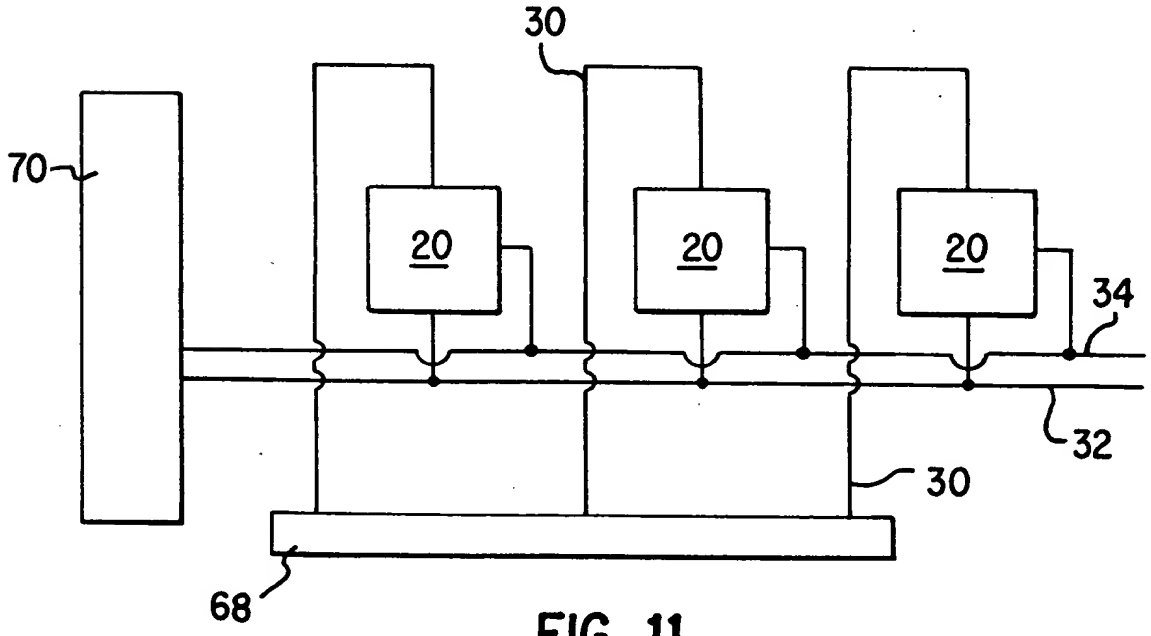

FIG. 11

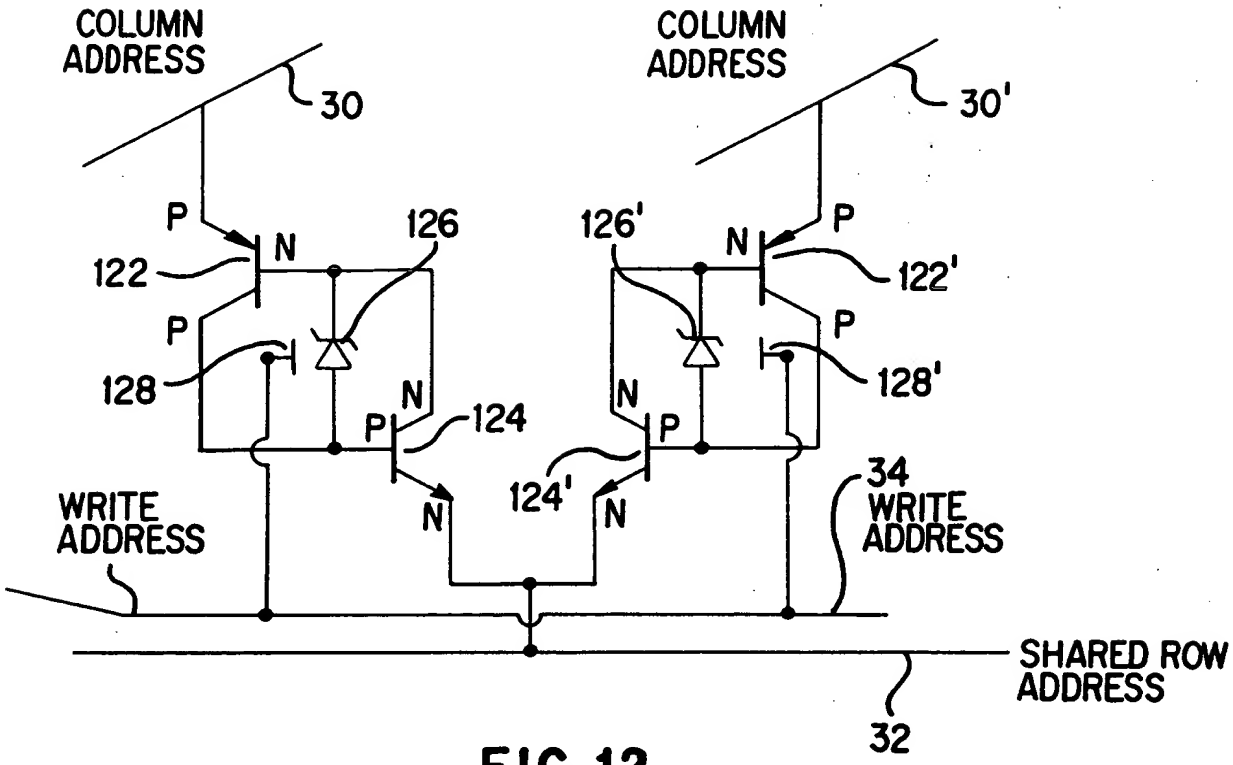
COLUMN ADDRESS
30
COLUMN ADDRESS
30'
P
N
126
122
P
128
N
P
124
N
126'
N
P
122'
P
128'
N
P
124'
N
WRITE ADDRESS
34
WRITE ADDRESS
SHARED ROW ADDRESS
32

FIG. 12

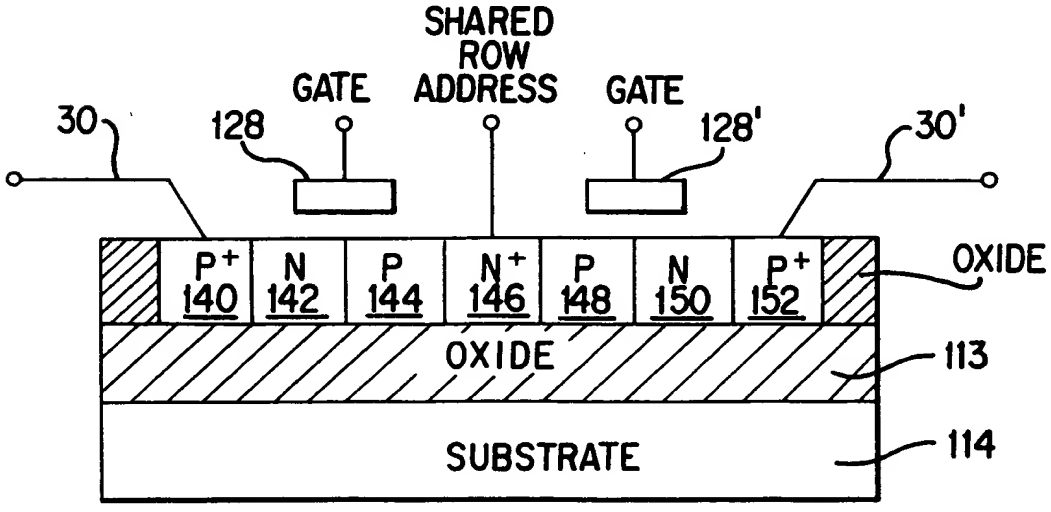
SHARED ROW ADDRESS
GATE
GATE
30
128
128'
30'
P+ 140
N 142
P 144
N+ 146
P 148
N 150
P+ 152
OXIDE
OXIDE
113
SUBSTRATE
114

FIG. 13

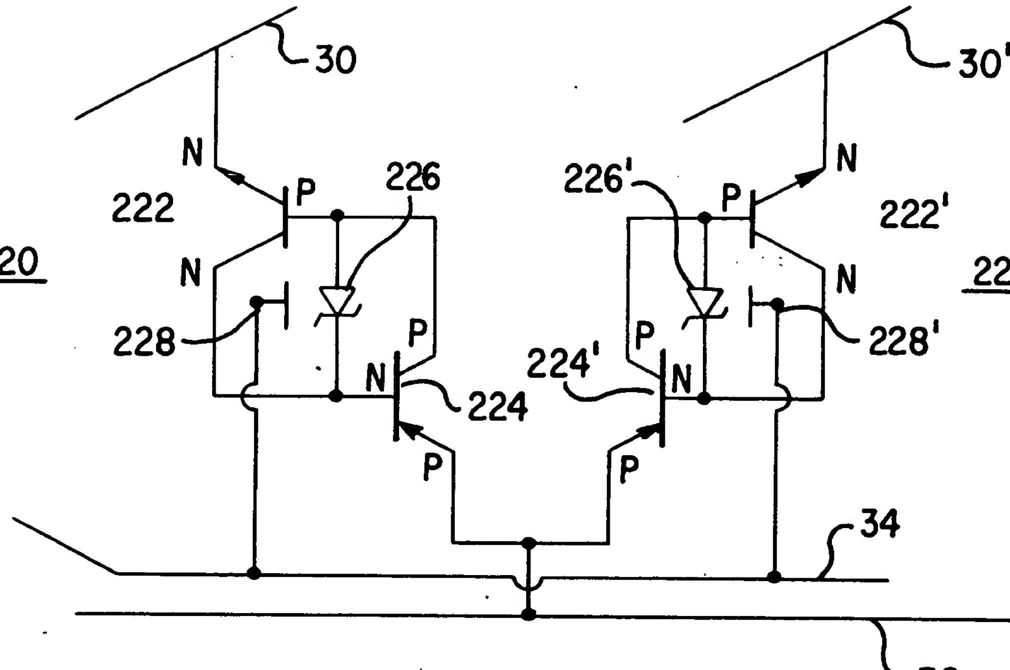
30
30'
N
P
226
226'
P
N
222
222'
220
220'
N
N
228
228'
P
P
N
224'
N
224
P
P
34
32

FIG. 15

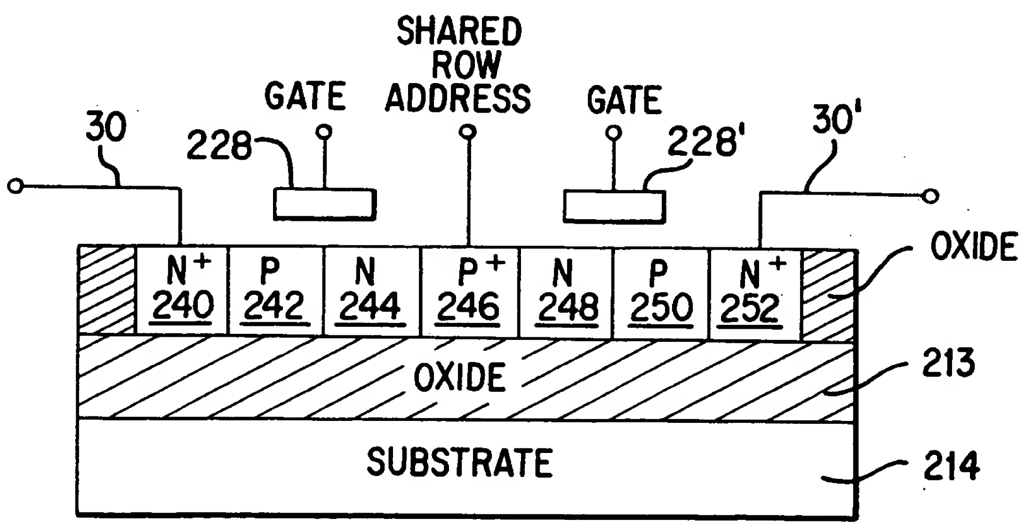
SHARED
ROW
ADDRESS
GATE
GATE
30
228
228'
30'
N+
240
P
242
N
244
P+
246
N
248
P
250
N+
252
OXIDE
OXIDE
213
SUBSTRATE
214

FIG. 16